7 Coders and Multiplexers

In this chapter, we will look two types of operations that are common in digital devices: coding and multiplexing. Coding devices can be categorised as either encoders or decoders and similarly, we have multiplexers and de-multiplexers. Commonly available ICs will be used to illustrate these operations.

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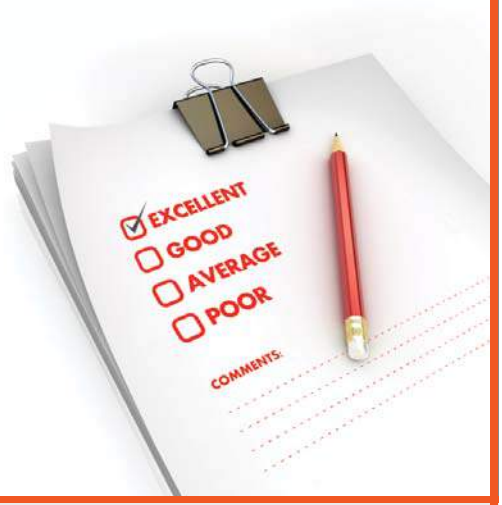

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7.1 Encoder

An encoder is a device that does some form of coding, for example converting an octal number to binary as shown in Figure 7.1. In general, a N bit encoder has 2^N input lines and N output lines; in the case of octal to binary encoder, it is 8-to-3, i.e. eight input lines and three output lines. Only one input is active[10] at a time.

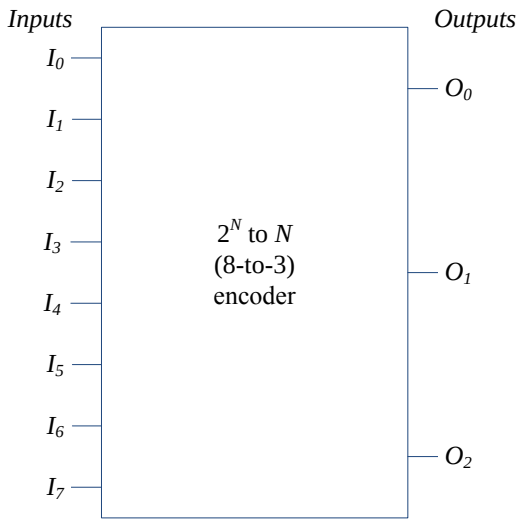

Figure 7.1: A general encoder example: octal to binary.

Table 7.1 gives the truth table for this encoder. It can be seen that only one input line is active. For simplicity of discussion at this stage, we assume that the input and output lines for the decoder are ACTIVE HIGH, though we will see later that most decoders have ACTIVE LOW input and output lines. When one input is activated, the corresponding binary is the output. For example, when $I_6 = 1$, the outputs are $O_2 = 1$, $O_1 = 1$ and $O_0 = 0$, which is binary number for six. Note the ordering of the indexes for the input and output lines in Table 7.1: $I_7, I_6,\ldots,I_0$ are ordered from left to right while it is O_2,O_1,O_0 for the outputs. This ordering scheme is just chosen to allow easier understanding of the concepts.

10 Either ACTIVE LOW or ACTIVE HIGH, to be discussed later.

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Table 7.1: Truth table for a general 8-to-3 encoder

Inputs								*Outputs*		
I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_2	O_1	O_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

7.1.1 Priority encoding

Though only one input line is supposed to be active at a given time, it is possible to have multiple lines being active perhaps due to noise or error in the logic design. To avoid unpredictable output in such situations, priority encoding can be utilised. Priority encoders allow the higher indexed input lines to take precedence over the lower indexed pins.

Consider a 4-to-2 encoder with the truth table as shown in Table 7.2. Whenever the higher indexed input line is active, the lower indexed lines do not have any effect (irrespective of being active or not). For example, when $I_3 = 1$, the logic values for I_0, I_1 and I_2 do not affect the output (shown by don't care conditions X) and the output will $O_1 = 1$ and $O_0 = 1$.

Table 7.2: Truth table for a general 4-to-2 priority encoder (with don't care conditions)

Inputs				*Outputs*	
I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

The K-maps for outputs O_0 and O_1 are as shown in Figure 7.2. However, the don't care conditions now appear for the inputs, which is different to the don't care conditions for the outputs that was studied in Chapter 4. In order to complete the K-maps, we have to expand Table 7.2 to include both the 0 and 1 cases for the don't care conditions as shown in Table 7.3. From the K-maps, the expressions for the outputs are

$$O_0 = \overline{I_2} I_1 + I_3,$$

$$O_1 = I_2 + I_3.$$

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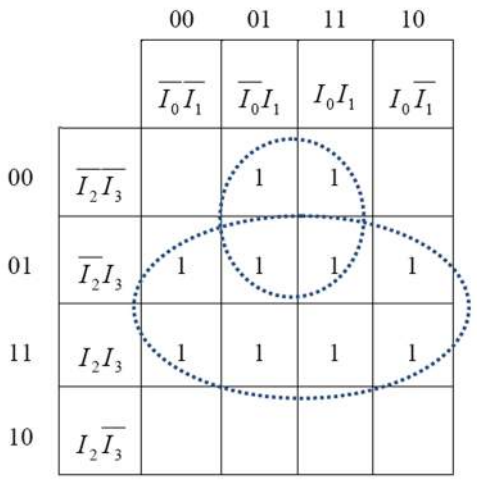
From Table 7.3, we can also note that the outputs will be all logic 0 for two cases: when all inputs are 0 and $I_0 = 1$. This ambiguity can be solved by using a special output pin and will be discussed later.

Table 7.3: Truth table for a general 4-to-2 priority encoder (showing full don't care cases)

Inputs				*Outputs*	
I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Figure 7.3 shows the logic circuits for the outputs O_0 and O_1.



(a)

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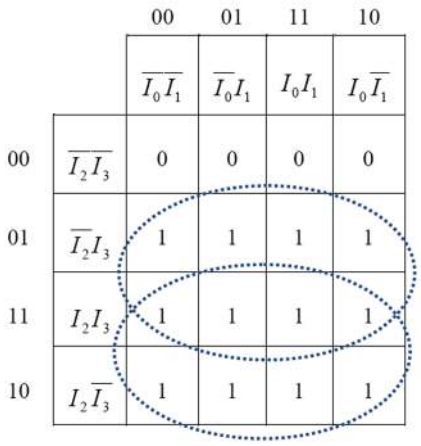

(b)

Figure 7.2: K-maps for 4-to-2 priority encoder: (a) O_0 (b) O_1.

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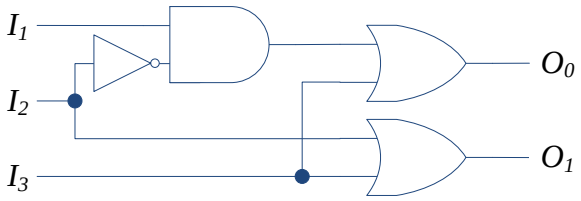

Figure 7.3: Logic circuit for 4-to-2 priority encoder.

7.1.2 Enable inputs

Figure 7.4 shows a 8-to-3 encoder IC, 74xx148 with pin configurations[11]. Both the inputs and outputs are ACTIVE LOW, i.e. enabled/activated on logic 0. It is also a priority encoder, so the higher indexed inputs take priority.

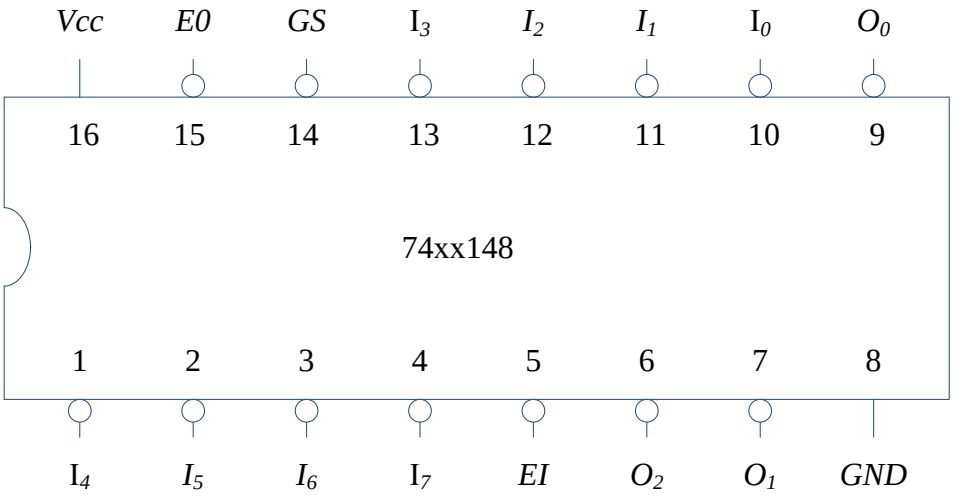

Figure 7.4: 8-to-3 encoder IC, 74xx148 pin configuration.

Table 7.4 shows the truth table and it can be seen that there are additional input and outputs: Enable Input ($\overline{EI}$), Enable Output ($\overline{EO}$) and Group Select ($\overline{GS}$). All the enable pins are also ACTIVE LOW as shown by the overbars in Table 7.4 and by the presence of bubbles in Figure 7.4. $\overline{EI}$ enables the device and allows the input values to change the outputs. As shown in Table 7.4, when $\overline{EI} = 1$, the outputs are all inactive (i.e. logic 1). When $\overline{EI} = 0$, the inputs are enabled and affects the outputs. For example, when $\overline{I_7} = 0$, the outputs are $\overline{O_2} = \overline{O_1} = \overline{O_0} = 0$. Similarly when $\overline{I_3} = 0$, the outputs are $\overline{O_2} = 1$ and $\overline{O_1} = \overline{O_0} = 0$ (note that the outputs are active low, so it represents 3 in binary).

11 xx denotes different types of ICs available such as low power Schottky version, 74LS148 and high speed CMOS version, 74HC148.

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When all the inputs are inactive, $\overline{GS}$ is disabled ($\overline{GS}=1$) and when any one input is active, then $\overline{GS}=0$. Hence $\overline{GS}$ is useful to indicate whether the condition $\overline{O_2}=\overline{O_1}=\overline{O_0}=1$ is caused by $\overline{I_0}=0$ or if all inputs are inactive.

$\overline{EO}$ is used when cascading several encoders to form a larger priority encoding system. For this purpose, $\overline{EO}$ output is connected $\overline{EI}$ input of the lower priority encoder.

Table 7.4: Truth table for 74xx148

Inputs									*Outputs*				
$\overline{EI}$	$\overline{I_7}$	$\overline{I_6}$	$\overline{I_5}$	$\overline{I_4}$	$\overline{I_3}$	$\overline{I_2}$	$\overline{I_1}$	$\overline{I_0}$	$\overline{O_2}$	$\overline{O_1}$	$\overline{O_0}$	$\overline{GS}$	$\overline{EO}$
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	X	X	X	X	X	X	X	0	0	0	0	1
0	1	0	X	X	X	X	X	X	0	0	1	0	1
0	1	1	0	X	X	X	X	X	0	1	0	0	1
0	1	1	1	0	X	X	X	X	0	1	1	0	1
0	1	1	1	1	0	X	X	X	1	0	0	0	1
0	1	1	1	1	1	0	X	X	1	0	1	0	1
0	1	1	1	1	1	1	0	X	1	1	0	0	1
0	1	1	1	1	1	1	1	0	1	1	1	0	1

7.2 Decoder

Decoder is the opposite of encoder, for example a 3-to-8 decoder that accepts three binary inputs and activates the corresponding single output as shown in Figure 7.5. Figure 7.6 shows a 74xx138 IC, which is binary-to-octal (3-to-8) decoder. The three inputs are active HIGH (note that there is no bubble in the figure) but the eight outputs are all ACTIVE LOW. In addition, three enable inputs: two ACTIVE LOW and one ACTIVE HIGH need to be in the asserted mode to enable the IC (i.e. $E_3=1$, $\overline{E_2}=0$ and $\overline{E_1}=0$). If any of these inputs are in an inactive state, then all the outputs will be in inactive state (i.e. logic 1 since these are ACTIVE LOW pins) irrespective of the inputs as shown by the first three rows in Table 7.5. When E_3, $\overline{E_2}$ and $\overline{E_1}$ are enabled, the inputs affect the output. For example when $I_2=I_1=I_0=1$ then pin $\overline{O_7}$ becomes low and when $I_2=I_1=1$ and $I_0=0$ then pin $\overline{O_6}$ becomes low.

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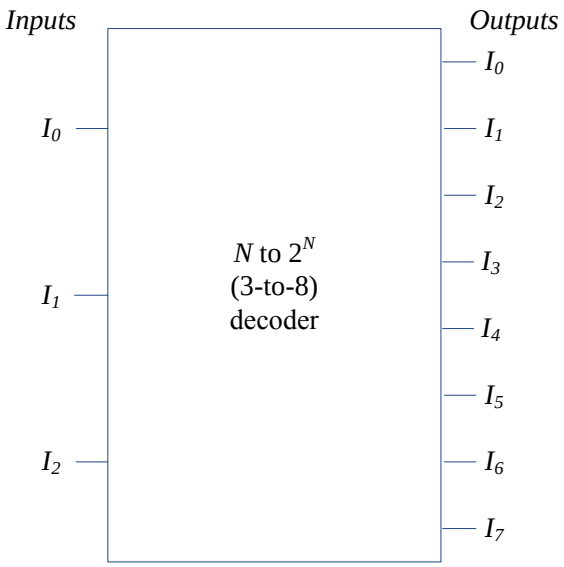

Figure 7.5: 3-to-8 decoder example.

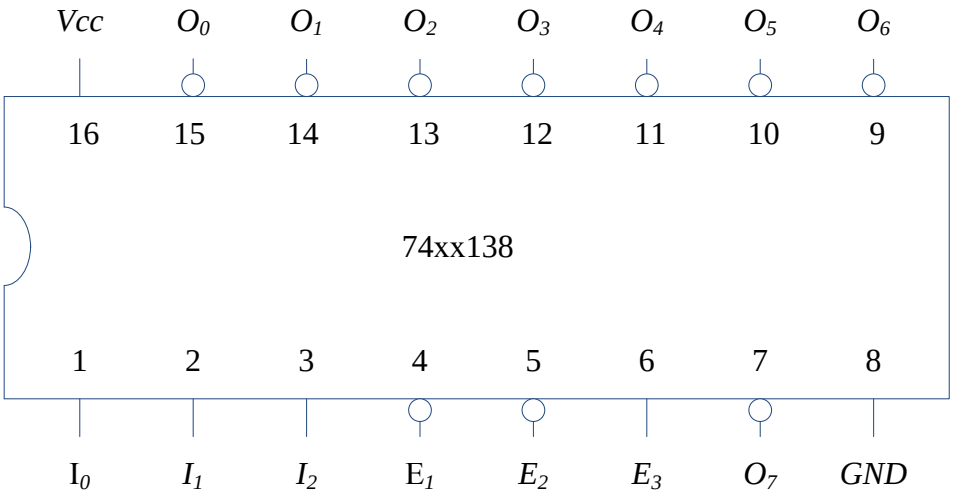

Figure 7.6: 3-to-8 encoder IC, 74xx138 pin configuration.

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Table 7.5: Truth table for 74xx138

Inputs						*Outputs*							
E_3	$\overline{E_2}$	$\overline{E_1}$	I_2	I_1	I_0	$\overline{O_7}$	$\overline{O_6}$	$\overline{O_5}$	$\overline{O_4}$	$\overline{O_3}$	$\overline{O_2}$	$\overline{O_1}$	$\overline{O_0}$
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

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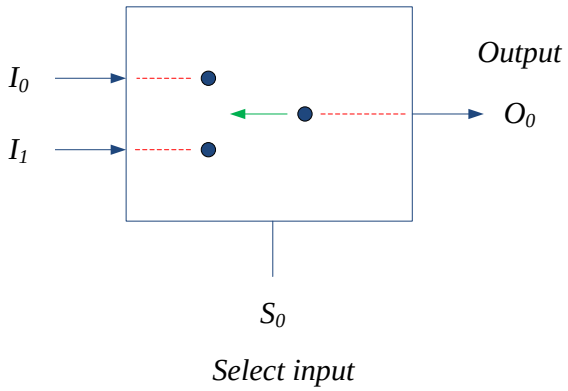
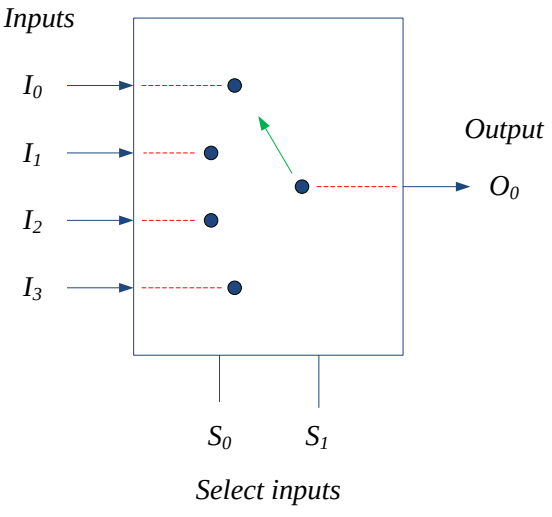
7.3 Multiplexer

Multiplexer (also known as data selector) is a digital device that acts like a switch taking several inputs and connecting a selected input to the output at a time. Simple two input and four input multiplexers are shown in Figure 7.7. For the two input multiplexer, there are two inputs: I_1 and I_0 with one output, O_0. The selector input, S_0 will decide the route from input to the output. For example, when $S_0 = 1$, I_1 is selected and data at I_1 is routed to output O_0. For the four input multiplexer, there are four inputs: I_3, I_2, I_1 and I_0 with one output, O_0. The selector inputs, S_1 and S_0 will decide which connection is made from the input to the output. For example, when $S_1 = S_0 = 1$, I_3 is selected and data at I_3 is routed to output O_0. Tables 7.6 and 7.7 show the truth table for these multiplexers.



(a)



(b)

Figure 7.7: Simple multiplexers (a) two inputs (b) four inputs.

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Table 7.6: Truth table for two input multiplexer

Select input S_0	*Output*
0	$O_0 = I_0$
1	$O_0 = I_1$

Table 7.7: Truth table for four input multiplexer

Select inputs		*Output*
S_1	S_0	
0	0	$O_0 = I_0$
0	1	$O_0 = I_1$
1	0	$O_0 = I_2$
1	1	$O_0 = I_3$

To obtain the logic circuit diagram for two input multiplexer, truth table as in Table 7.8 should be constructed. With this, K-map for output O_0 can be obtained as shown in Figure 7.8. Two pair loops can be drawn to give the output as

$$O_0 = \overline{S_0} I_0 + S_0 I_1.$$

The logic circuit diagram is given in Figure 7.9. Similar approach could be utilised to obtain logic circuit diagrams for higher input multiplexers.

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Table 7.8: Full truth table for two input multiplexer

S_0	I_0	I_1	O_0
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

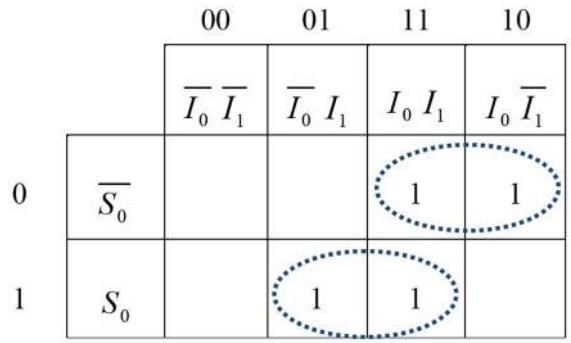

Figure 7.8: K-map for two input multiplexer.

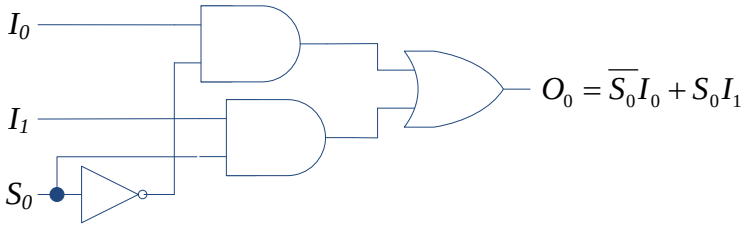

Figure 7.9: Logic circuit diagram for two input multiplexer.

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7.3.1 Multiplexer IC example

A quadruple 2-line to 1-line multiplexer (IC 74xx157) is shown in Figure 7.10. The IC contains two sets of four inputs (I_{0a}, I_{1a}, I_{2a}, I_{3a} and I_{0b}, I_{1b}, I_{2b}, I_{3b}) that can be routed to the four outputs (O_0, O_1, O_2, O_3) depending on the select input, S_0. The enable, $\overline{E}$ input must asserted, i.e. it must be logic 0 for the IC to be enabled. Table 7.9 gives the truth table for this IC. When $S_0 = 0$, the outputs follow I_{0a}, I_{1a}, I_{2a}, I_{3a} inputs and when $S_0 = 1$, the outputs follow I_{0b}, I_{1b}, I_{2b}, I_{3b} inputs.

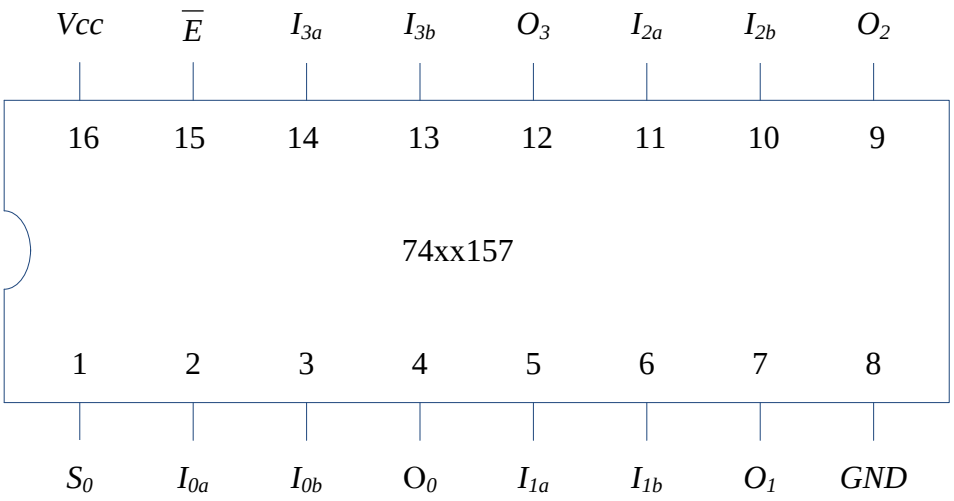

Figure 7.10: Quadruple 2-line to 1-line multiplexer IC, 74xx157 pin configuration.

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Table 7.9: Truth table for 74xx157

$\overline{E}$	S_0	O_0	O_1	O_2	O_3
1	X	0	0	0	0
0	0	I_{0a}	I_{1a}	I_{2a}	I_{3a}
0	1	I_{0b}	I_{1b}	I_{2b}	I_{3b}

7.4 De-multiplexer

A de-multiplexer does the opposite of multiplexer in that it takes a single input and distributes it to a selected output. Hence it is also known as data distributor. An example of 1-line to 8-line demultiplexer is shown in Figure 7.11.

IC 74xx138, which is a 3-to-8 decoder (that we discussed earlier) can also be used as a 1-line to 8-line demultiplexer by using $\overline{E_1}$ as data input and the three inputs as selectors. The other two enable pins are asserted to enable the IC by connecting $\overline{E_2}$ to ground (i.e. logic 0) and E_3 is connected to *Vcc* (+5 V) to give logic 1. Using this convention, the pin configuration is as shown in Figure 7.12 and the truth table as in Table 7.10. The select inputs (S_0, S_1, S_2) will select the particular output pin and the input data (I_0) will be distributed to this selected output pin. Due to the dual mode nature of such ICs, these are usually known as *decoder/demultiplexer* ICs.

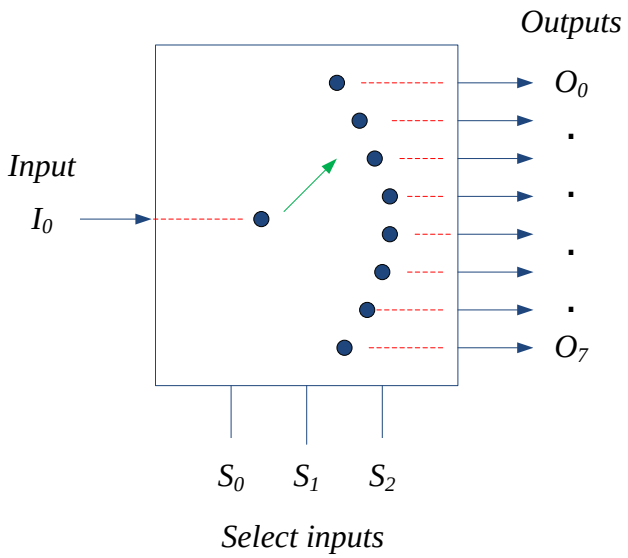

Figure 7.11: 1-line to 8-line demultiplexer.

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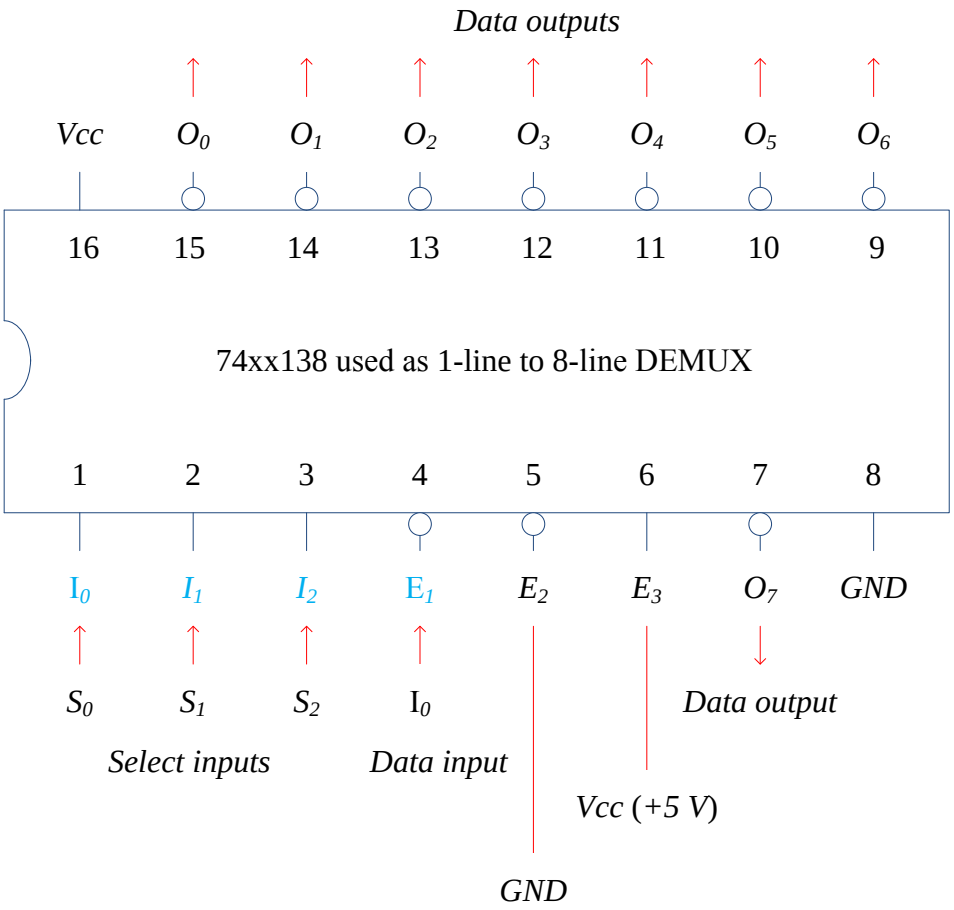

Figure 7.12: 1-line to 8-line demultiplexer using 74xx138 decoder.

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Table 7.10: Truth table for 1-line to 8-line demultiplexer (using 74xx138 IC)

Select inputs			*Outputs*							
S_2	S_1	S_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	1	1	1	1	1	1	1	I_0
0	0	1	1	1	1	1	1	1	I_0	1
0	1	0	1	1	1	1	1	I_0	1	1
0	1	1	1	1	1	1	I_0	1	1	1
1	0	0	1	1	1	I_0	1	1	1	1
1	0	1	1	1	I_0	1	1	1	1	1
1	1	0	1	I_0	1	1	1	1	1	1
1	1	1	I_0	1	1	1	1	1	1	1

It should be remembered that 74xx138 IC has outputs that are ACTIVE LOW, hence inactive outputs have logic 1 as shown in Table 7.10.

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